PCF85116-3

2048 × 8-bit CMOS EEPROM with I²C-bus interface

Rev. 03 — 19 August 2002 **Product data**

1. Description

The PCF85116-3 is an 16 kbits (2048 × 8-bit) floating gate Electrically Erasable Programmable Read Only Memory (EEPROM). By using redundant EEPROM cells it is fault tolerant to single bit errors. In most cases multi bit errors are also covered. This feature dramatically increases reliability compared to conventional EEPROM memories. Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Only one PCF85116-3 device is required to support all eight blocks of 256 × 8-bit each.

Timing of the E/W cycle is carried out internally, thus no external components are required. A write-protection input at pin 7 (WP) allows disabling of write-commands from the master by a hardware signal. When pin 7 is HIGH, data in the EEPROM are protected. The data bytes received will not be acknowledged by the PCF85116-3 and the EEPROM contents are not changed.

Remark: The PCF85116-3 is pin and address compatible to the PCx85xxC-2 family. The PCF85116-3 covers the whole address space of 16 kbits; address inputs are no longer needed. Therefore, pins 1 to 3 are not connected. The write-protection input (WP) is on pin 7.

2. Features

- Low power CMOS:
  - maximum operating current 1.0 mA
  - maximum standby current 10 μA (at 5.5 V), typical 4 μA
- Non-volatile storage of 16 kbits organized as eight blocks of 256 × 8-bit each
- Single supply with full operation down to 2.7 V
- On-chip voltage multiplier
- Serial input/output I²C-bus (100 kbits/s standard-mode and 400 kbits/s fast-mode)
- Write operations: multi byte write mode up to 32 bytes
- Write-protection input
- Read operations:
  - sequential read
  - random read
- Internal timer for writing (no external components)
- Power-on-reset
- High reliability by using redundant EEPROM cells

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- Endurance: 1000000 Erase/Write (E/W) cycles at T_{amb} = 22 °C
- 20 years non-volatile data retention time (minimum)
- Pin and address compatible to the PCx85xxC-2 family
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Offered in DIP and SO packages

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		2.7	-	5.5	V
I_{DDR}	supply current read	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	-	-	1.0	mA
I_{DDW}	supply current E/W	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	-	-	1.0	mA
I_{stb}	standby supply current	V_{DD} = 2.7 V	-	-	6	µA
		V_{DD} = 5.5 V	-	-	10	µA

4. Ordering information

Table 2: Ordering information

Type number		Package		
	North America	Name	Description	Version
PCF85116-3P	PCF85116-3N	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF85116-3T	PCF85116-3D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

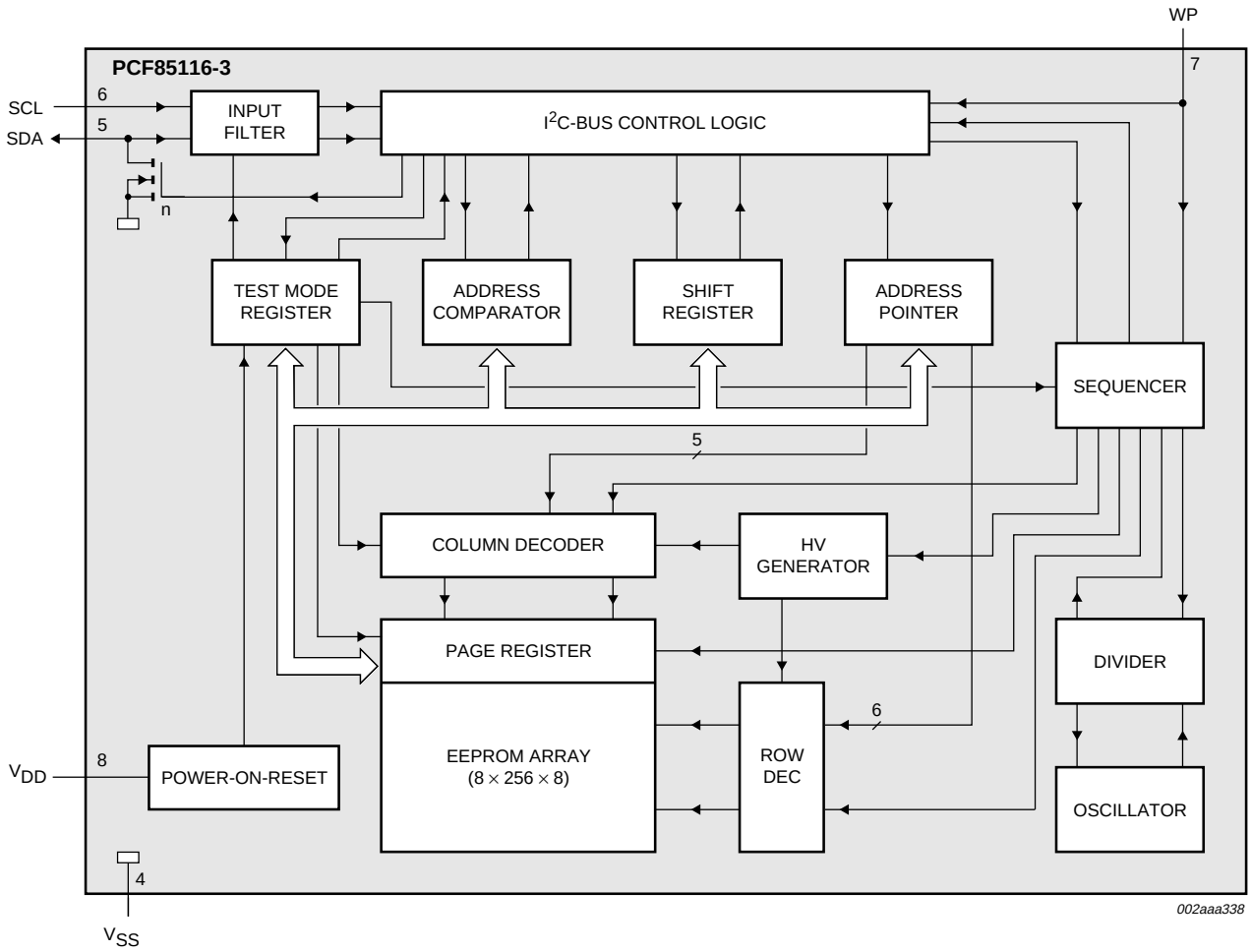


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

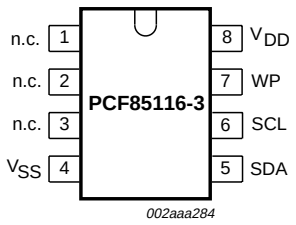


Fig 2. Pin configuration.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
n.c.	1	not connected
n.c.	2	not connected
n.c.	3	not connected
V_{SS}	4	negative supply voltage
SDA	5	serial data input/output (I^2C-bus)
SCL	6	serial clock input (I^2C-bus)
WP	7	active HIGH write-protection input
V_{DD}	8	positive supply voltage

7. Device selection

Table 4: Device selection code

Selection	Device code				Chip enable			R/$\overline{W}$
Bit	B7[1]	B6	B5	B4	B3	B2	B1	B0
Device	1	0	1	0	MEM SEL 2	MEM SEL 1	MEM SEL 0	R/$\overline{W}$

[1] The Most Significant Bit (MSB) ‘B7’ is sent first.

8. Functional description

8.1 I²C-bus protocol

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines; one for data signals (SDA), and one for clock signals (SCL).

Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

8.1.1 Bus conditions

The following bus conditions have been defined:

Bus not busy — Both data and clock lines remain HIGH.

Start data transfer — A change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the START condition.

Stop data transfer — A change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the STOP condition.

Data valid — The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

8.1.2 Data transfer

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is limited to 32 bytes in the E/W mode.

Data transfer is unlimited in the read mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate), a high-speed mode (100 kHz clock rate) and a fast speed mode (400 kHz clock rate) are defined. The PCF85116-3 operates in all three modes.

By definition, a device that sends a signal is called a ‘transmitter’, and the device which receives the signal is called a ‘receiver’. The device which controls the signal is called the ‘master’. The devices that are controlled by the master are called ‘slaves’.

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master generation of the STOP condition.

8.1.3 Device addressing

Following a START condition, the bus master must output the address of the slave it is accessing. The four MSBs of the slave address are the device type identifier (see Figure 3). For the PCF85116-3 this is fixed to ‘1010’.

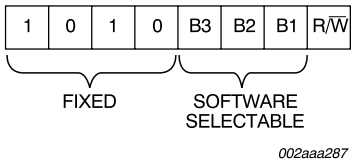


Fig 3. Slave address.

The next three significant bits of the slave address field (B3, B2, B1) are the block selection bits. It is used by the host to select one out of eight blocks (1 block = 256 bytes of memory). These are, in effect, the three most significant bits of the word address.

The last bit of the slave address (R/$\overline{W}$) defines the operation to be performed. When R/$\overline{W}$ is set to logic 1, a read operation is selected.

8.1.4 Write operations

Byte/word write: For a write operation, the PCF85116-3 requires a second address field. This address field is a word address providing access to any one of the eight blocks of memory. Upon receipt of the word address, the PCF85116-3 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a STOP condition.

After this STOP condition, the E/W cycle starts and the bus is free for another transmission. Its duration is a maximum of 10 ms.

During the E/W cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

Page write: The PCF85116-3 is capable of a 32-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit up to 32 data bytes within one transmission. After receipt of each byte, the PCF85116-3 will respond with an acknowledge. The master terminates the transfer by generating a STOP condition. The maximum total E/W time in this mode is 10 ms.

After the receipt of each data byte, the six high-order bits of the memory address providing access to one of the 64 pages of the memory remain unchanged. The five low-order bits of the memory address will be incremented only (see Figure 4). By these five bits a single byte within the page in access is selected. By an increment the memory address may change from 31 to 0, from 63 to 32, etc. If the master transmits more than 32 bytes prior to generating the STOP condition, data within the addressed page may be overwritten and unpredictable results may occur. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

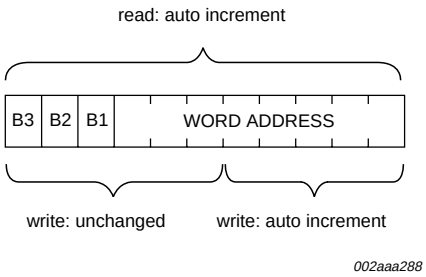


Fig 4. Auto-increment of memory address.

Remark: Write accesses to the EEPROM are enabled if the pin WP is LOW. When WP is HIGH the EEPROM is write-protected and no acknowledge will be given by the PCF85116-3 when data is sent. However, an acknowledge will be given after the slave address and the word address.

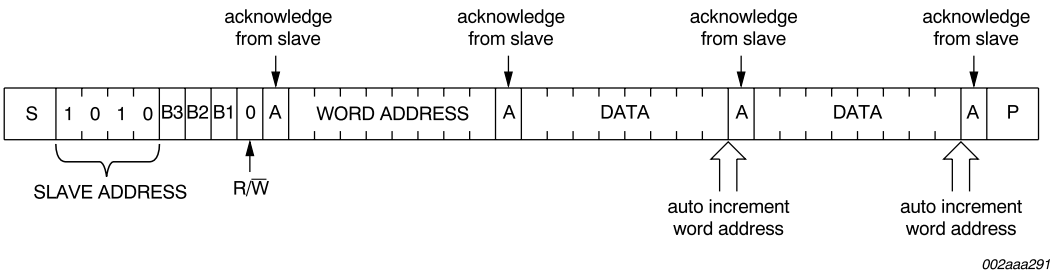


Fig 5. Auto increment memory address; two byte write.

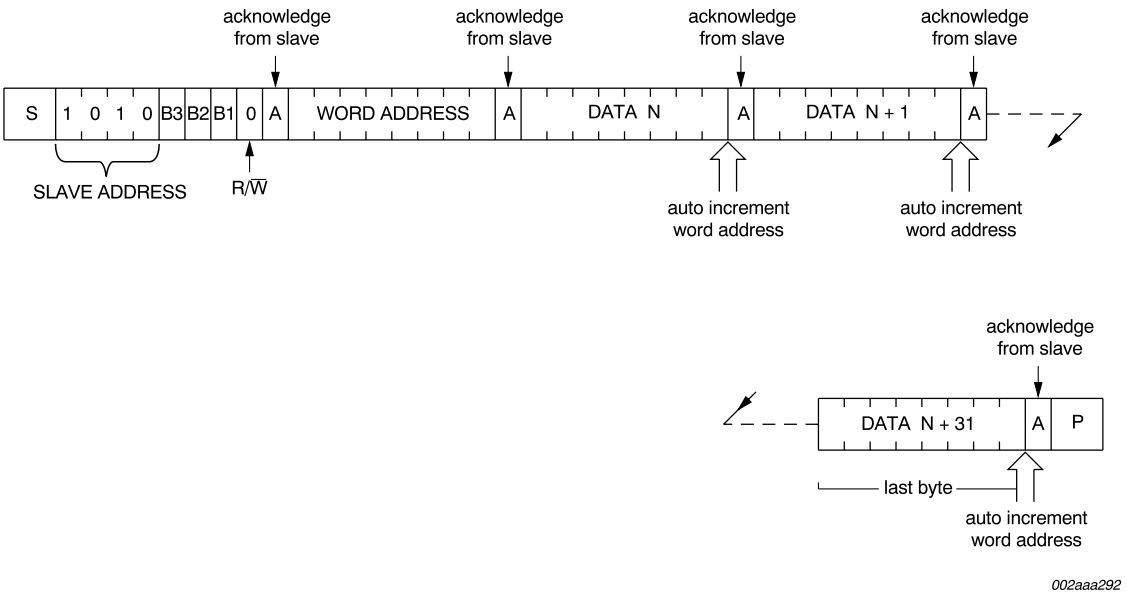


Fig 6. Page write operation; 32 bytes.

8.1.5 Read operations

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address (R/$\overline{W}$) is set to logic 1.

There are three basic read operations: current address read, random read, and sequential read.

Remark: During read operations all bits of the memory address are incremented after each transmission of a data byte. Contrary to write operations, an overflow of the memory address occurs from 2047 to 0 (see Figure 8).

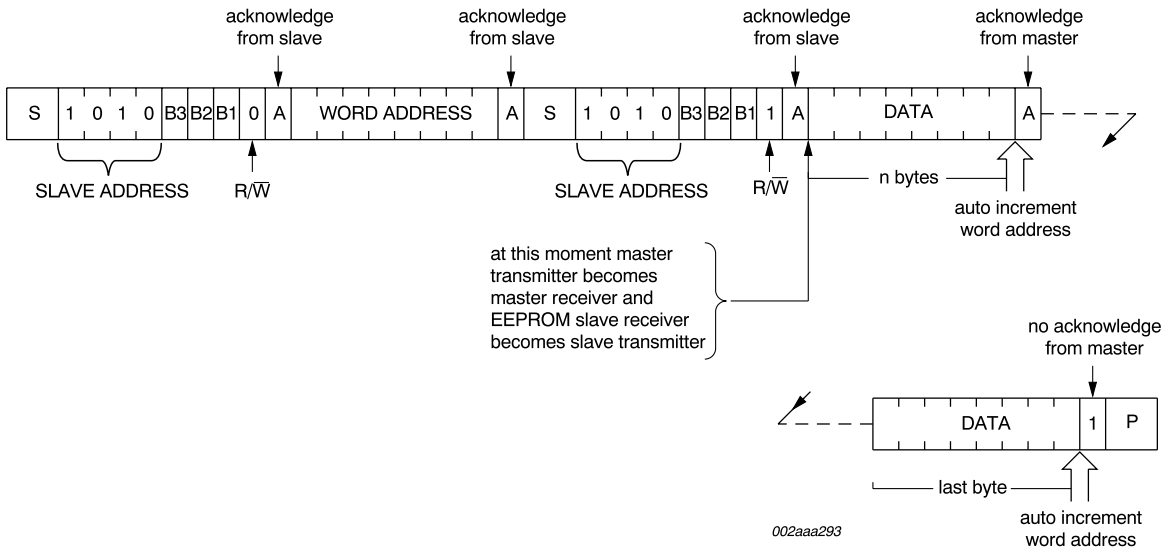


Fig 7. Master reads PCF85116-3 slave after setting word address (write word address; read data); sequential read.

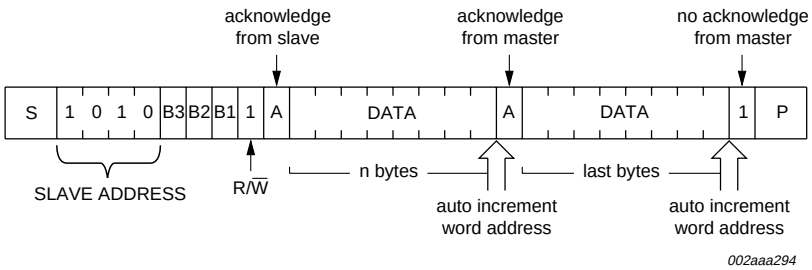


Fig 8. Master reads PCF85116-3 immediately after first byte (read mode); current address read.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+6.5	V
V_i	input voltage on any input pin	$\|Z_i\| > 500\ \Omega$	$V_{SS} - 0.8$	+6.5	V
I_i	input current on any input pin		-	1	mA
I_o	output current		-	10	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{esd}	electrostatic discharge voltage	[1]	2	-	kV

[1] ESD human body model Q22 at T_{amb} = 22 °C; discharge procedure according to MIL-STD-883C Method 3015.

10. Characteristics

Table 6: Characteristics

V_{DD} = 2.7 to 3.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		2.7	-	5.5	V
I_{DDR}	supply current read	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	-	-	1.0	mA
I_{DDW}	supply current E/W	f_{SCL} = 400 kHz; V_{DD} = 5.5 V	-	-	1.0	mA
$I_{DD(stb)}$	standby supply current	V_{DD} = 2.7 V	-	-	6	µA
		V_{DD} = 5.5 V	-	-	10	µA
SDA input/output (pin 5)						
V_{IL}	LOW level input voltage		−0.8	-	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	-	+6.5	V
V_{OL1}	LOW level output voltage	I_{OL} = 3 mA; $V_{DD(min)}$	-	-	0.4	V
V_{OL2}		I_{OL} = 6 mA; $V_{DD(min)}$	-	-	0.6	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	-	-	1	µA
$t_{o(f)}$	output fall time from V_{IHmin} to V_{ILmax}	[1]				
	with up to 3 mA sink current at V_{OL1}		$20 + 0.1C_b$	-	250	ns
	with up to 6 mA sink current at V_{OL2}		$20 + 0.1C_b$	-	250	ns
t_{SP}	pulse width of spikes suppressed by filter		0	-	100	ns
C_i	input capacitance	$V_I = V_{SS}$	-	-	10	pF
SCL input (pin 6)						
V_{IL}	LOW level input voltage		−0.8	-	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	-	+6.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	-	-	±1	µA
f_{SCL}	clock input frequency		0	-	400	kHz
t_{SP}	pulse width of spikes suppressed by filter		0	-	100	ns
C_i	input capacitance	$V_I = V_{SS}$	-	-	7	pF
WP input (pin 7)						
V_{IL}	LOW level input voltage		−0.8	-	$0.1V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.9V_{DD}$	-	V_{DD} + 0.8	V
Data retention time						
t_S	data retention time	T_{amb} = 55 °C	20	-	-	years

[1] The bus capacitance ranges from 10 to 400 pF (C_b = total capacitance of one bus line in pF).

11. I²C-bus characteristics

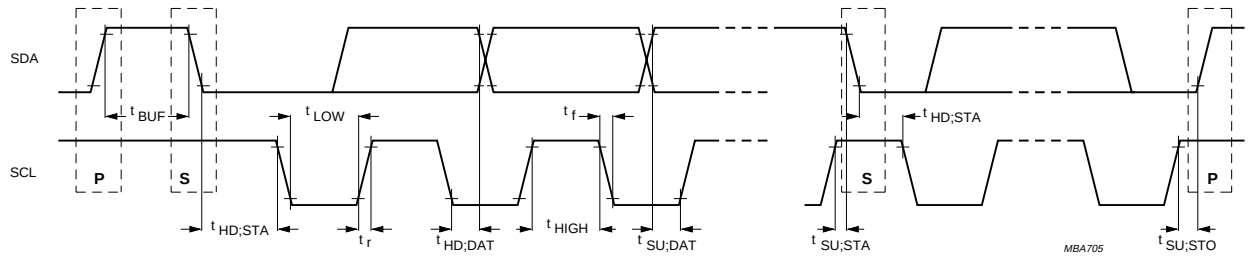
Table 7: I²C-bus characteristics

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}; see Figure 9.

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	clock frequency		0	100	0	400	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	-	1.3	-	µs
$t_{HD;STA}$	START condition hold time after which first clock pulse is generated		4.0	-	0.6	-	µs
t_{LOW}	LOW level clock period		4.7	-	1.3	-	µs
t_{HIGH}	HIGH level clock period		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for START condition	repeated start	4.7	-	0.6	-	µs
$t_{HD;DAT}$	data hold time						
	for CBUS compatible masters		5	-	-	-	µs
	for I²C-bus devices	[1]	0	-	0	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_r	SDA and SCL rise time		-	1000	$20 + 0.1C_b$[2]	300	µs
t_f	SDA and SCL fall time		-	300	$20 + 0.1C_b$[2]	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs

[1] The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.

[2] C_b = total capacitance of one bus line in pF.



P = STOP condition; S = START condition.

Fig 9. Timing requirements for the I²C-bus.

12. Write cycle limits

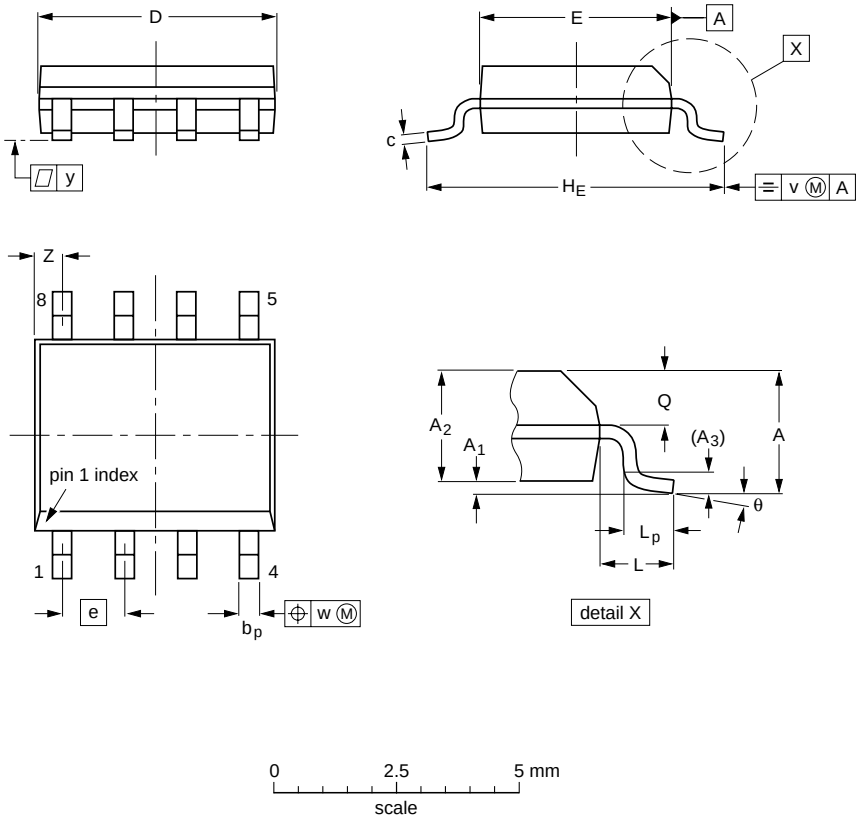
Table 8: Write cycle limits

The power-on-reset circuit resets the I²C-bus logic with a set-up time of ≤10 µs. Enabling the chip is achieved by connecting the WP input to V_{SS}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E/W cycle timing						
$t_{E/W}$	E/W cycle time		-	-	10	ms
Endurance						
$N_{E/W}$	E/W cycle per byte	T_{amb} = −40 to +85 °C	100000	-	-	cycles
		T_{amb} = 22 °C	1000000	-	-	cycles

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

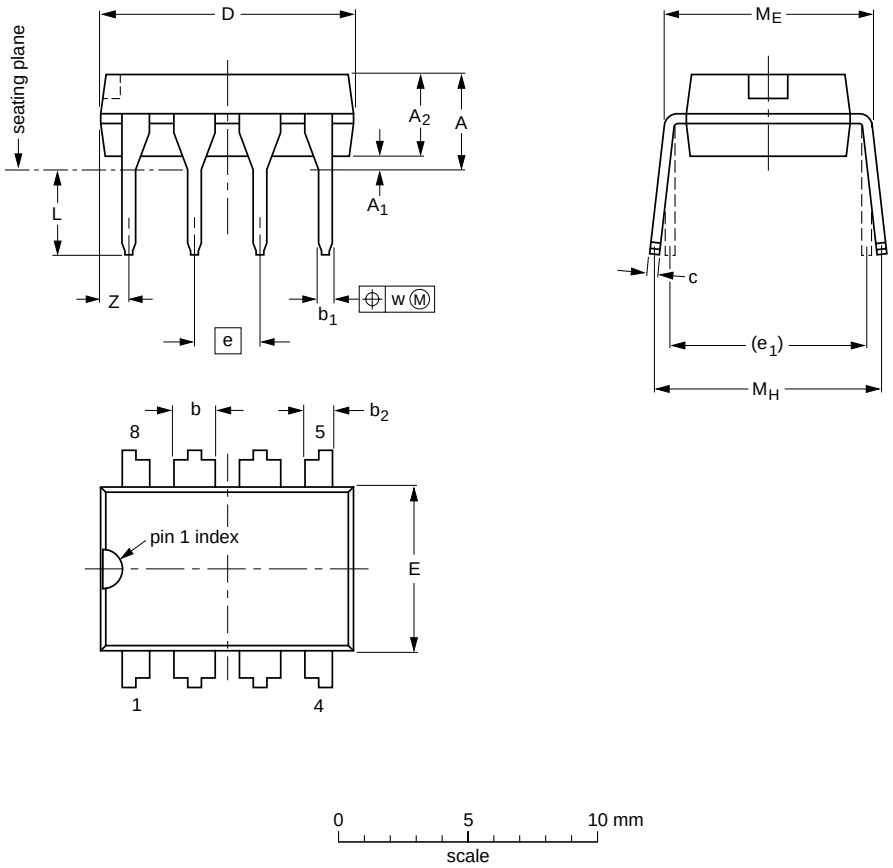
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

Fig 10. SO8 (SOT96-1).

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

Fig 11. DIP8 (SOT97-1).

14. Soldering

14.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Surface mount packages

14.2.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

14.2.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.2.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.3 Through-hole mount packages

14.3.1 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 9: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package[1]	Soldering method		
		Wave	Reflow[2]	Dipping
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable[3]	–	suitable
Surface mount	BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable	–
	HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable	–
	PLCC[5], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended[5][6]	suitable	–
	SSOP, TSSOP, VSO	not recommended[7]	suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15. Revision history

Table 10: Revision history

Rev	Date	CPCN	Description
03	20020819	-	**Product data (9397 750 10249); Engineering Change Notice 853-2356 28772; supersedes data in data sheet *PCF85116-3_2* dated 1997 Apr 02 (9397 750 01994).** Modifications: • The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard. • Table 2 on page 2: North America type numbers added. • Figure 1 on page 3: modified. • Table 3 on page 4: description for pin 7 (WP) adjusted. • Figures 3, 4, 5, 6, 7, 8: modified to display fixed and software-selectable slave addresses.

16. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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Contact information

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